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Effect of Heating on ICs Performance in Embedded Systems

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Abstract

Chip temperature is increasing with continued technology scaling due to increased power density and decreased device feature sizes. Since temperature has significant impact on performance and reliability, accurate thermal and circuit analysis are of great importance. Due to the shrinking device feature size, effects occur at the nanometer scale, such as ballistic transport of energy carriers and electron tunneling, have become increasingly important and must be considered. However, many existing thermal and circuit analysis methods are not able to consider these effects efficiently, if at all. This thesis presents methods for accurate and efficient multi-scale thermal and circuit analysis. For circuit analysis, the simulation of single electron device circuits is specifically studied.

Interconnect is one of the main performance determinant of modern integrated circuits (ICs). The new technology of vertical ICs places circuit blocks in the vertical dimension in addition to the conventional horizontal plane. Compared to the planar ICs, vertical ICs have shorter latencies as well as lower power consumption due to shorter wires. This also increases speed, improves performances and adds to ICs density.

Keywords: *ICs, MTTF, Security, Attacks, Tamper Mechanisms.*

Introduction

The technological revolution that started with the introduction of the transistor just over half a century ago is without parallel in the way it has shaped our economy and our daily lives. The current trend toward nano scale electronics is expected to have a similar impact into the third millennium. Commercial integrated circuits are currently available with transistors whose smallest lateral feature size is less than 100 nm and the thinnest material films are below 2 nm, or only a few atomic layers thick. Such miniaturization has led to tremendous integration levels, with a hundred million transistors assembled together on a chip area no larger than a few square centimeters. Integration levels are projected to reach the giga scale as the smallest lateral device feature sizes approach 10 nm. With the demand for high-performance integrated circuits, there has been an escalation of power dissipation and heat flux at the silicon level. This has resulted in a greater impact of substrate and metal line temperatures on the reliability and performance of devices and interconnections. Today's semiconductor devices are chiefly being motivated by the "smaller and faster" demands because they generally mean higher performance. Consequently, the ULSI chips have been pushed to higher clock speed and packaging density. The higher clock speed results in higher power consumption and the increase in packaging density results in large power density (power per unit area). For example, the power density of high-performance microprocessors has already reached 50W/cm² at the 100nm technology node [1] and will soon reach 100W/cm² [2]. A direct impact of increasing power density is the dramatic on-chip temperature rise which translates into reduced reliability. The temperature Difference between the heat source and surrounding ambient causes heat to flow out of the system. It is this temperature difference which causes the energy flow. If heat is not removed at a rate equal to or greater than its rate of generation, junction temperatures will rise.

Higher junction temperatures reduce mean time to failure (MTTF) for the devices. Device reliability has a direct impact on the overall system reliability. Removing heat from these

devices is thus a major task facing design engineers of modern electronic systems concerned with improving reliability. Understanding the effect of heat on the reliability of electronic products and the integrity of manufacturing processes is critical if failures are to be avoided. This means the need to understand thermal management and modeling techniques and the need for comprehensive data has never been greater.

The operating temperature is a function of power or power density. Nevertheless, power density itself cannot be used as a proxy for temperature, i.e. power density modeling cannot replace temperature modeling because temperature fluctuation is not simply proportional to the power consumption, neither the power density. There are other factors that significantly impact temperature distribution [3] in space and time that are also needed to be taken care of. These factors include heat spreading and temporal and spatial temperature filtering effects. Heat spreading occurs when heat flows from a smaller surface area to a larger surface area. Temporal temperature filtering is attributed to the long thermal time constant of silicon and package which tends to filter out fast changes in power and power density. Temperature filtering can also happen spatially where the power and power density change over a small dimension (high spatial frequency). All these effects can be modeled by solving the heat diffusion equation. Therefore, temperature must be modeled directly in order to perform accurate thermal analysis during the design process.

Some General Aspects of Heat Conduction

The energy given up by the constituent particles such as atoms, molecules, or free electrons of the hotter regions of a body to those in cooler regions is called heat. Conduction is the mode of heat transfer in which energy exchange takes place in solids or in fluids in rest (i.e. no convection motion resulting from the displacement of the macroscopic portion of the medium) from the region of high temperature to the region of low temperature due to the presence of temperature gradient in the body. The heat flow cannot be measured directly, but the concept has physical meaning because it is related to the measurable scalar quantity called temperature. Therefore, once the temperature distribution T(r,t) within a body is determined as a function of position and time, then the heat flow in the body is readily computed from the laws relating heat flow to the temperature gradient.

The science of heat conduction is principally concerned with the determination of temperature distribution within solids. The basic law that gives the relationship between the heat flow and the temperature gradient, based on experimental observations, is generally named after the French mathematical physicist Joseph Fourier, who used it in his analytic theory of heat. For a homogeneous, isotropic solid (i.e. material in which thermal conductivity is independent of direction) the Fourier law is given in the form

$$q(r,t) = -\kappa \nabla T(r,t) \quad W/m^2 \qquad (1)$$

Where the temperature gradient is a vector normal to the isothermal surface, the heat flux vector q(r,t) represents heat flow per unit time, per unit area of the isothermal surface in the direction of the decreasing temperature, and κ is called the thermal conductivity of the material which is a positive, scalar quantity. Since the heat flux vector q(r,t) points in the direction of decreasing temperature, a minus sign Is included in Eq. (1) to make the heat flow a positive quantity. When the heat flux is in W/m and the temperature gradient is in C/m, the thermal conductivity κ has the units W/(m C). Clearly, the heat flow rate for a given temperature gradient is directly proportional to the thermal conductivity κ of the material. Therefore, in the analysis of heat conduction, the thermal conductivity of the material is an important property, which controls the rate of heat flow in the medium. There is a wide difference in the thermal conductivities of various engineering materials. The highest value is given by pure metals and the lowest value by gases and vapors; the amorphous insulating materials and inorganic liquids have thermal conductivities that lie in between. Thermal conductivity also varies with temperature. For most pure metals it decreases with temperature, whereas for gases it increases

with increasing temperature At nanometer length scales, the familiar continuum Fourier law for heat conduction is expected to fail due to both classical and quantum size effects (Geppert, 1999; Zeng et al., 2003; Majumdar, 1993). The past two decades have seen increasing attention to thermal conductivity and heat conduction in nanostructures. Experimental methods for characterizing the thermal conductivity of thin films and nanowires have been developed and are still evolving. Experimental data have been reported on various nanostructures: thin films, super lattices, nanowires, and nanotubes. Along the way, models and simulations have been developed to explain the experimental data. This section summarizes some past work and the current understanding of heat conduction in nanostructures. We first give a brief overview on the fundamental physics that distinguishes phonon heat conduction in nanostructures from that in macrostructures. Then we discuss a few size effects in nanostructures that impact their thermal conductivity.

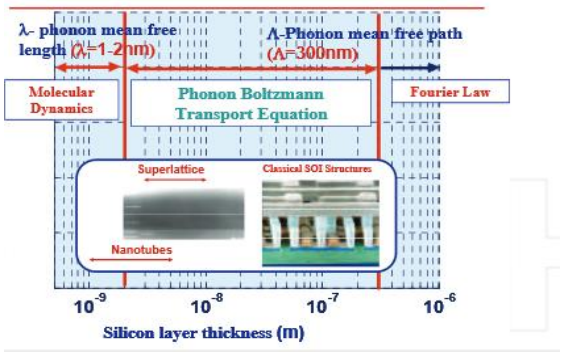

Figure (1)

Fig(1) Regime map for phonon transport in ultra-thin silicon layers. Mean free path Λ is a distance that phonons travel on average before being scattered by other phonons. If the dimension of the silicon layer is smaller than Λ, the Boltzmann Transport Equation (BTE) should be used for heat transfer analysis of the thin film. The dominant phonon wavelength, λ, at room temperature, is on the order of 2-3 nm. Analogous phonon wave simulations should be performed for devices with thicknesses comparable to λ[4].

Joule Heating

Joule heating occurs when an electrical current is passed through a material and the material's resistivity causes heat generation. Joule heating effects are common in devices and circuits where the heat generated by a current may be an important influence. For example, the ability to predict how electrical current will affect temperature distribution is useful when analyzing performance parameters of MEMS or electronic devices[3].

Joule Heating in IC Packages

Heat is generated from the silicon active surface due to two factors—active switching and leakage. All the energy consumed by the integrated circuit is first dissipated in the form of heat in the transistors and interconnects, and are eventually removed to the environment by heat transfer. While power, P, is the rate of energy consumption, heat generation rate (or heat dissipation rate), Q, is the amount of heat generated or dissipated in unit amount of time. In this dissertation, sometimes when we use "heat", what we really mean is the heat generation rate. The actual meaning usually can be told from the context.

Temperature Effect on Circuit Performance Metris

Temperature has a direct and often substantial impact on nearly all of the key figures of merit (performance parameters) of a VLSI circuit, including circuit speed, lifetime, power dissipation, and power plane integrity. The chip temperature is in turn set by the power dissipation in the substrate and interconnects as well as the physical layout, routing resources, and power distribution network in the chip[7].

Full-Chip Temperature Calculation

Heat is generated in both the substrate and the interconnections. The major source of heat generation is the power dissipation of devices

that are embedded in the substrate. Some power dissipation also results from Joule heating (or self-heating) caused by the flow of current in the interconnect network. Although interconnect Joule heating constitutes only a small fraction of the total power dissipation in the chip, the temperature rise in the interconnections due to Joule heating can be significant. This is due to the fact that interconnects are located away from the Silicon substrate and the heat sink by several layers of insulating materials which have lower thermal conductivities than that of Silicon.Simply stated, the operating temperature of a VLSI chip can be calculated from the following linear equation:

$$T_{chip} = T_a + R_\theta \cdot \frac{P_{tot}}{A}$$

where Tchip is the average chip (silicon junction) temperature, Ta is the ambient temperature (Ta = 25°C), Ptot(in W) is the total power consumption, A (in cm2) is the chip area, and Rθ is the equivalent thermal resistance of the substrate (Si) layer plus the package and heat sink (cm2°C/W.) As this equation shows, to calculate the chip temperature, one must have calculated power dissipation of the circuit (Ptot), constructed the chip thermal model (Rθ), and be given information about the environment (Ta). The self-heating effect can be analyzed as follows [6]. The metal temperature, Tmetal, is given by

$$T_{metal} = T_{chip} + \Delta T_{self}$$

$$\Delta T_{self} = R_E \, I_{rms}^2 R_{\theta,self}$$

where ΔTself is the temperature rise of the metal interconnect due to the flow of current, RE is the electrical resistance of interconnect, and Rθ, self is the thermal impedance of the interconnect line to the substrate.

Effect on Power Dissipation

As stated previously, temperature has a strong effect on sub threshold leakage, which tends to be a major component of the circuit power dissipation in sub-90 nm CMOS designs (At 90-nm-process nodes, leakage accounts for 25 to 40% of total power. At 65-nm-processes, leakage accounts for 50 to 70% of total power.) Since leakage is critically dependent on operating temperature and power supply, the authors of [8] present a full chip leakage estimation technique which accurately accounts for power supply and temperature variations. State of the art techniques are used to compute the thermal and power supply profile of the entire chip. Closed-form models are presented which relate leakage to temperature and VDD variations. These models coupled with the thermal and VDD profile is used to generate an accurate full chip leakage estimation technique considering environmental variations. The results of this approach are demonstrated on large-scale industrial designs.

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